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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO. CONFIRMATION NO		
09/612,971	07/10/2000	Jae-seong Shim	1293.1128/MJB	9406	
21171 7.	590 08/08/2003		•		
STAAS & HALSEY LLP SUITE 700 1201 NEW YORK AVENUE, N.W.			EXAMINER TU, CHRISTINE TRINH LE		
			2133		
			DATE MAILED: 08/08/2003 -		

Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary		Applicati n	No.	Applicant(s)	`/				
		09/612,971		SHIM ET AL.	·				
		Examiner		Art Unit					
		Christine T.		2133					
The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply									
A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication. - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely. - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication. - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). - Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b). Status									
1)🖂	Responsive to communication(s) filed on	<u>09 July 2003</u> .							
2a) <u></u>	This action is FINAL . 2b)⊠	This action is n	on-final.						
3)□	3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213. Disposition of Claims								
·		٠٠							
	Claim(s) 1-39 is/are pending in the application.								
i	4a) Of the above claim(s) <u>32 and 33</u> is/are withdrawn from consideration.								
l	Claim(s) 35-39 is/are allowed.								
l	6) Claim(s) 1-31 and 34 is/are rejected.								
l	7) Claim(s) is/are objected to.								
8) Claim(s) are subject to restriction and/or election requirement. Application Papers									
9) The specification is objected to by the Examiner.									
10)☐ The drawing(s) filed on is/are: a)☐ accepted or b)☐ objected to by the Examiner.									
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).									
11) The proposed drawing correction filed on is: a) approved b) disapproved by the Examiner.									
If approved, corrected drawings are required in reply to this Office action.									
12)☐ The oath or declaration is objected to by the Examiner.									
Priority under 35 U.S.C. §§ 119 and 120									
13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).									
a)[a) All b) Some * c) None of:								
	1. Certified copies of the priority documents have been received.								
	Certified copies of the priority documents have been received in Application No								
* S	Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received.								
14) <u></u> □ A	cknowledgment is made of a claim for don	nestic priority und	er 35 U.S.C. § 119(e	e) (to a provisional	application).				
a) ☐ The translation of the foreign language provisional application has been received. 15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.									
Attachment									
2) D Notice	e of References Cited (PTO-892) e of Draftsperson's Patent Drawing Review (PTO-948 nation Disclosure Statement(s) (PTO-1449) Paper No	3) 5		(PTO-413) Paper Not Patent Application (PTo					
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Page 2

Application/Control Number: 09/612,971

Art Unit: 2133

- 1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.
- 2. Claims 29-31 and 34 are again rejected under 35 U.S.C. § 101 because the claimed invention is directed to non-statutory subject matter.

The claim invention is recited with data (which is an error correction block structure) embodied on a computer readable medium (which is an optical disk). However, the data does not provide functionality to either the data as claimed or to the optical disk. As such, the claimed invention is recited with non-functional descriptive material, i.e., mere data. Non-functional descriptive material stored on a computer readable medium is merely carried on the medium, it is not structurally and functionally interrelated to the medium.

3. Claims 1-18 and 34 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

a.Claim 1:

At line 11, the phrase "wherein a burst error is corrected in an HD-DVD" is <u>not</u> interrelated with any of the previously recited steps of obtaining a plurality of inner parity blocks, generating e-byte PI for each of the plurality of PI blocks, generating f-byte outer parity (PO) in a PO direction of the error correction block. In other words, the phrase is <u>not coherent</u> with the previously recited steps.

Art Unit: 2133

b.Claims 2-18:

These claims are rejected because they depend on claim(s) 1 and contain the same problems of indefiniteness.

c.Claim 34:

This claim cannot depend on a canceled claim (claim 33).

- 4. The following rejections are based on the best understanding of the claimed invention by the examiner in view of the ambiguities that exist in the claims as mentioned above (supra ¶ 3).
- 5. Claims 1-6, 15-16 19-27, 29, 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuroda et al. (6,252,383 and Kuroda hereinafter).

Claim 1:

Kuroda discloses the invention substantially as claimed. Kuroda teaches (figures 1A & 1B) an error correcting process for generating an ECC block from a data structure. The data structure is segmented into a plurality of data sectors (20). Each section (20) is firstly divided into plural blocks each of which is 172 bytes data (figure 1B) and each divided data is arranged in a vertical direction. At this time, the data blocks (33) are arranged in 12 lines in the vertical direction (column 5 lines 27-50).

Kuroda also teaches that for each data block (33) arranged in the vertical direction, ECC internal code (PI) (31) having 10 bytes data is affixed to the end of the data block (33) to constitute one correction block (34). At this stage, the ECC internal codes (31) (PIs) are affixed and

Art Unit: 2133

arranged in the vertical direction. After that, this process is repeated with respect to 16 data sectors (20) (column 5 lines 51-59).

Kuroda further teaches that the correction block (34) of 192 lines are divided in the vertical direction from the beginning thereof, for each one byte, in the state that the 192 Ines of the correction blocks (34) are arranged in the vertical direction. 16 ECC external codes (PO) (32) are affixed to each of the vertically divided data blocks, It is noted that ECC external code (PO) (32) is also affixed to a portion of the ECC internal code (PI) (31) within the correction block (34) (column 5 lines 60-57).

Kuroda does not explicitly teach the features of generating PIs and POs. It would have been obvious to one having ordinary skill in the art at the time the invention was made to realize that Kuroda's error correcting process would have been comprised of the features of generating the POs and POs. The artisan would have been motivated to realize so because Kuroda teaches that each of the PIs and each of the POs is being obtained and affixed to the end of a data block (33) and a vertically divided data blocks, respectively (column 5 lines 51-67).

Kuroda does not explicitly teach that a burst error is corrected in an HD-DVD. Kuroda, however, teaches that the error correcting process in the DVD-R of this embodiment an and ECC block serving as an error correction unit (column 5 lines 27-30). It would have been obvious to one skilled in the art to realize that Kuroda's error correcting process does not exclude the inclusive of burst error correction. In other words, Kuroda's error correcting processing can include many different types of error correcting processes including a burst error correcting process.

Art Unit: 2133

Claims 2-6 and 16:

Kuroda does not explicitly teach (n/x) + e > 256, $(n+e) \times (m+f) < 64K$, n=688 and m=96, x=172 and e=8, nor f=12. It would have been obvious to one having ordinary skill in the art at the time the invention was made to realize that Kuroda's value of variables m, n x, e and f would have been quality the situations above. The artisan would have been motivated to do so because choose the values of m, n, x, e and f would have been obvious of design choice for the size of each data

sector and size of each ECC block to accommodate the error correction.

Claim 15:

Kuroda teaches that a data sector comprises 4-byte ID, 2-byte IEC, 6-byte RSV, 2048-byte data, and 4-byte EDC (figure 1A).

Claims 19-22:

Kuroda discloses the invention substantially as claimed. Kuroda teaches (figures 1A & 1B) an error correcting process for generating an ECC block from a data structure. The data structure is segmented into a plurality of data sectors (20). Each section (20) is firstly divided into plural blocks each of which is 172 bytes data (figure 1B) and each divided data is arranged in a vertical direction. At this time, the data blocks (33) are arranged in 12 lines in the vertical direction (column 5 lines 27-50).

Kuroda also teaches that for each data block (33) arranged in the vertical direction, ECC internal code (PI) (31) having 10 bytes data is affixed to the end of the data block (33) to constitute one correction block (34). At this stage, the ECC internal codes (31) (PIs) are affixed and

Art Unit: 2133

arranged in the vertical direction. After that, this process is repeated with respect to 16 data sectors (20) (column 5 lines 51-59).

Kuroda further teaches that the correction block (34) of 192 lines are divided in the vertical direction from the beginning thereof, for each one byte, in the state that the 192 Ines of the correction blocks (34) are arranged in the vertical direction. 16 ECC external codes (PO) (32) are affixed to each of the vertically divided data blocks, It is noted that ECC external code (PO) (32) is also affixed to a portion of the ECC internal code (PI) (31) within the correction block (34) (column 5 lines 60-57).

Kuroda does not explicitly teach the features of generating PIs and POs. It would have been obvious to one having ordinary skill in the art at the time the invention was made to realize that Kuroda's error correcting process would have been comprised of the features of generating the POs and POs. The artisan would have been motivated to realize so because Kuroda teaches that each of the PIs and each of the POs is being obtained and affixed to the end of a data block (33) and a vertically divided data blocks, respectively (column 5 lines 51-67).

Claims 23-27:

Kuroda teaches that an encoder (9) affixes the ECC internal code (PI) (31) and ECC external code (PO) (32) to constitute the ECC block (30) including the interleave process to the ECC block (30) (column 8 lines 14-18).

Art Unit: 2133

Claims 29-31 and 34:

Kuroda teaches a ECC block is being recorded on a DVD wherein the DVD is a high density optical disc and the like. The ECC block comprises inner parities (PIs) and external parities (POs) that are affixed and arranged in the vertical direction and in the horizontal direction (figures 1A & 1B, column 1 lines 7-13, column 6 lines 13-33 and column 5 lines 27-67).

6. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kuroda in view of Ozaki et al. (4,719,628).

Claim 17:

Kuroda does not teach the Galois Field operation. Ozaki teaches that Galois field GF (2^m) can be used in error correction method.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to use Ozaki's Galois Field method in Kuroda's error correcting process. One having ordinary skill in the art would be motivated to combine the teachings of Kuroda and Ozaki because both references teach error correction for data information.

7. Claim 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kuroda (6,252,838) in view of Hoshino (5,586,108).

Claim 28:

Kuroda does not teach the feature of interleaving quantity of the data in relation to the size of a burst error. Hoshino, however, teaches that the length of burst error correction of data is increased by interleaving error correction code among the sectors (abstract, lines 8-10).

Art Unit: 2133

It would have been obvious to one having ordinary skill in the art at the time the invention was made to Kuroda's interleaving feature would have considered the burst error correction as taught by Hoshino. One having ordinary skill in the art would be motivated to combine the teachings of Kuroda and Hoshino because both of the references teach an error correction method being used in a disk recording medium.

8. Applicant's arguments filed on July 9, 2003 have been fully considered but they are not persuasive.

For claims 29-31 and 34, applicant states that the encoding of the data in a structure meets the requirements of 35 U.S.C. §101. However, applicant should realize that in the body of claim 1, what is being claimed is "an error correction block structure...., a plurality of inner parity blocks..., a plurality of f-byte outer parities...". Base the language of the claim, error correction block structure is being encoded. In other words, the error correction block structure (itself) does not provide any encoding function. Therefore, none of the error correction block structure, the plurality of inner parity blocks, the plurality of f-byte outer parities provides any encoding function. Hence claims 29-34 is still rejected as non-statutory.

Applicant argues that the prior art's design cannot correct burst error in an HD-DVD. Examiner traverses applicant's remark. Firstly, applicant should noted that the recited phrase "burst error is corrected in an HD-DVD" is not interrelated with any of the above steps (as being rejected in paragraph 3 above). Secondly, Kuroda teaches the error correcting process in the DVD-R of the embodiment and an ECC block serving as an error correction unit (column 5 lines

Application/Control Number: 09/612,971

Art Unit: 2133

27-30). It would have been obvious to one skilled in the art to realize that Kuroda's error correcting process does not exclude the inclusive of burst error correction.

Page 9

As per claim 4, applicant argues that Kuroda does not teach that n is 688 and m is 96. As stated above in paragraph 5, choosing the value of m and n would have been a matter of design choice. The artisan would have been motivated to do so because choosing the values of m and n would have been obvious of design choice for the size of each data sector and size of each ECC block to accommodate the error correction.

- 9. Claims 7-14 and 18 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include <u>all of the limitations of the base claim and any intervening claims</u>.
- 10. Claims 35-39 are allowable over prior arts.
- 11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.
- 12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christine T. L. Tu whose telephone number is (703) 305-9689. The examiner can normally be reached on Monday to Thursday from 8:30 A.M. to 6:00 P.M.

 If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisors.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady, can be reached on (703) 305-9595.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Art Unit: 2133

13. Any response to this action should be mailed to:

Commissioner of Patents and Trademarks Washington, D.C. 20231

or faxed to:

(703) 746-7238 (for formal after-final communications intended for entry), (703) 746-7239 (for formal communications intended for entry),

Or:

(703) 746-7240 (for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA. 22202, Sixth Floor (Receptionist).

Christine T. L. Tu

Primary Patent Examiner

Art Unit 2133

August 6, 2003